


Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended): A probe card assembly for electrically communicating test data between a semiconductor test tester apparatus and a semiconductor device under test, said probe card assembly comprising:

 a substrate configured to electrically contact said semiconductor tester apparatus,
a plurality of probes configured to electrically contact said semiconductor device under test, said plurality of probes located to a first side of said substrate, and
a daughter card ~~secured~~ located to a second side of said substrate ~~in spaced relationship to said substrate~~, said daughter card being substantially coplanar to said substrate, there being a space between said daughter card and said substrate.

Claim 2 (original): The probe card assembly of claim 1 further comprising an electric circuit at least a portion of which is disposed on said daughter card.

Claim 3 (original): The probe card assembly of claim 2, wherein said electric circuit includes active circuit elements.

Claim 4 (original): The probe card assembly of claim 2, wherein said electric circuit is configured to enhance test capabilities of said semiconductor test apparatus.


Claim 5 (original): The probe card assembly of claim 2, wherein said electric circuit is configured to customize at least a portion of said test data to test needs of said semiconductor device under test.

Claim 6 (original): The probe card assembly of claim 5, wherein said test data comprises test signals generated by said semiconductor test apparatus and said electric circuit customizes at least a portion of said test signals.

Claim 7 (original): The probe card assembly of claim 5, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

Claim 8 (original): The probe card assembly of claim 1 further comprising a plurality of said daughter cards.

Claim 9 (original): The probe card assembly of claim 8, wherein said plurality of daughter cards are disposed in stacked relationship to each other.

 Claim 10 (original): The probe card assembly of claim 8 further comprising an electric circuit at least a portion of which is disposed on each of said plurality of daughter cards.

Claim 11 (original): The probe card assembly of claim 10, wherein said electric circuit includes active circuit elements.

Claim 12 (original): The probe card assembly of claim 10, wherein said electric circuit is configured to enhance test capabilities of said semiconductor test apparatus.

Claim 13 (original): The probe card assembly of claim 10, wherein said electric circuit is configured to customize at least a portion of said test data to test needs of said semiconductor device under test.

Claim 14 (original): The probe card assembly of claim 13, wherein said test data comprises test signals generated by said semiconductor test apparatus and said electric circuit customizes at least a portion of said test signals.


Claim 15 (original): The probe card assembly of claim 13, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

Claim 16 (original): The probe card assembly of claim 8, wherein said plurality of daughter cards includes at least three daughter cards.

Claim 17 (original): The probe card assembly of claim 16 further comprising an electric circuit at least a portion of which is disposed on each of said at least three daughter cards.

Claim 18 (original): The probe card assembly of claim 16, wherein said at least three daughter cards are disposed in stacked relationship to each other.

Claim 19 (currently amended): A method of making a probe card assembly, said method comprising:

 providing a substrate including a plurality of tester contacts,
~~securing~~ disposing a plurality of probes to a first side of said substrate, said probes configured to electrically contact a semiconductor device under test, and
~~securing~~ disposing a daughter card to a second side of said substrate ~~in spaced relationship to said substrate~~, said daughter card being substantially coplanar to said substrate, there being a space between said daughter card and said substrate.

Claim 20 (original): The method of claim 19 further comprising:

providing an electric circuit, and
disposing at least a portion of said electric circuit on said daughter card.

Claim 21 (original): The method of claim 20, wherein said electric circuit includes active circuit elements.


Claim 22 (original): The method of claim 20, wherein said electric circuit is configured to enhance test capabilities of said semiconductor test apparatus.

Claim 23 (original): The method of claim 20, wherein said electric circuit is configured to customize test data to test needs of said semiconductor device under test.

Claim 24 (original): The method of claim 23, wherein said test data comprises test signals to be input into said semiconductor device under test and said electric circuit customizes at least a portion of said test signals.

Claim 25 (original): The method of claim 23, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

Claim 26 (original): The method of claim 19 further comprising securing a plurality of said daughter cards to said substrate.

 Claim 27 (original): The method of claim 26 further comprising securing said plurality of daughter cards to said substrate in stacked relationship to each other.

Claim 28 (original): The method of claim 26 further comprising:
 providing an electric circuit, and
 disposing at least a portion of said electric circuit on each of said plurality of daughter cards.

Claim 29 (original): The method of claim 28, wherein said electric circuit includes active circuit elements.


Claim 30 (original): The method of claim 28, wherein said electric circuit is configured to enhance test capabilities of said semiconductor test apparatus.

Claim 31 (original): The method of claim 28, wherein said electric circuit is configured to customize test data to test needs of said semiconductor device under test.

Claim 32 (original): The method of claim 31, wherein said test data comprises test signals to be input into said semiconductor device under test and said electric circuit customizes at least a portion of said test signals.

Claim 33 (original): The method of claim 31, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

Claim 34 (original): The method of claim 26, wherein said plurality of daughter cards includes at least three daughter cards.



Claim 35 (original): The method of claim 34 further comprising:
providing an electric circuit, and
disposing at least a portion of said electric circuit on each of said at least three daughter cards.

Claim 36 (original): The method of claim 34 further comprising securing each of said at least three daughter cards to said substrate in stacked relationship to each other.

Claim 37 (original): A probe card assembly made using the process of claim 19.

Claim 38 (original): A probe card assembly made using the process of claim 20.

Claim 39 (original): A probe card assembly made using the process of claim 22.

Claim 40 (original): A probe card assembly made using the process of claim 26.

Claim 41 (original): A probe card assembly made using the process of claim 30.


Claim 42 (currently amended): A probe card assembly comprising:

printed circuit means for electrically communicating with a semiconductor tester apparatus,

contact means for electrically communicating with a semiconductor device under test, said contact means being secured to a first surface of said printed circuit means, ~~and~~

daughter card means for physically supporting at least a portion of an electric circuit, said daughter card means secured to a second surface of said printed circuit means and being substantially coplanar to said printed circuit means, and

an electric circuit, at least a portion of which is disposed on said daughter card means.



Claim 43 (original): The probe card assembly of claim 42, wherein said daughter card means comprises a plurality of daughter cards in stacked relationship to each other, each of said plurality of daughter cards being substantially coplanar to said printed circuit means.

Claim 44 (original): The probe card assembly of claim 43, wherein said plurality of daughter cards includes at least three daughter cards.

Claim 45 (original): The probe card assembly of claim 42, wherein said electric circuit comprises processing means for processing test data for testing said semiconductor device under test.

Claim 46 (original): The probe card assembly of claim 45, wherein said processing means enhances test capabilities of said semiconductor test apparatus.

Claim 47 (original): The probe card assembly of claim 45, wherein said processing means customizes said test data to meet test needs of said semiconductor device under test.

Claim 48 (original): The probe card assembly of claim 47, wherein said test data comprises test signals to be input into said semiconductor device under test and said processing means customizes at least a portion of said test signals.

Claim 49 (original): The probe card assembly of claim 47, wherein said test data comprises response signals generated by said semiconductor device under test and said processing means customizes at least a portion of said response signals.

Claim 50 (original): A probe card assembly for electrically communicating test data between a semiconductor test apparatus and a semiconductor device under test, said probe card assembly comprising:

- a printed circuit board configured to electrically contact said semiconductor tester apparatus,
- a plurality of probes configured to electrically contact said semiconductor device,
- a daughter card secured to said printed circuit board in spaced relationship to said printed circuit board, said daughter card being substantially coplanar to said printed circuit board, and
- an electric circuit configured to enhance test capabilities of said semiconductor test apparatus, at least a portion of said electric circuit being disposed on said daughter card.

Claim 51 (original): The probe card assembly of claim 50 further comprising a plurality of said daughter cards.

Claim 52 (original): The probe card assembly of claim 51, wherein said daughter cards are disposed in stacked relationship to each other.

Claim 53 (original): The probe card assembly of claim 51, wherein said plurality of daughter cards includes at least two daughter cards.

Claim 54 (original): The probe card assembly of claim 51, wherein said plurality of daughter cards includes at least three daughter cards.

Claim 55 (original): The probe card assembly of claim 50, wherein said electric circuit enhances test capabilities of said semiconductor test apparatus by processing at least a portion of said test data.

Claim 56 (original): The probe card assembly of claim 55, wherein said test data comprises test signals generated by said semiconductor tester apparatus and said electric circuit processes at least a portion of said test signals.

Claim 57 (original): The probe card assembly of claim 55, wherein said test data comprises response signals generated by said semiconductor device and said electric circuit processes at least a portion of said response signals.
